Entry of amdt filed 08-25-03 is approved. JLE

In the Claims:

1. (Original) An integrated circuit memory device, comprising:

a plurality of memory cells arranged as a plurality of blocks, each of the blocks including a plurality of primary memory cells that are coupled and decoupled to and from respective input/output lines responsive to a primary column select line and a plurality of redundant memory cells that are coupled and decoupled to and from respective ones of the input/output lines responsive to a redundant column select line;

a column select circuit, coupled to the primary column select lines and to the redundant column select lines, that drives a first primary column select line responsive to application of a first column address input and that drives a first redundant column select line in place of the first primary column select line responsive to application of a second column address input;

a plurality of sense amplifiers; and

an input/output control circuit configurable to selectively connect input/output lines to a sense amplifier such that a primary memory cell associated with the first primary column select line is coupled to the sense amplifier responsive to the first column address input and such that a redundant memory cell associated with the first redundant column select line is coupled to the sense amplifier responsive to the second column address input.

2. (Original) The device of Claim 1, wherein respective pluralities of input/output lines are associated with respective ones of the blocks of memory cells, wherein the first primary memory cell and the first redundant memory cell are in the same block of memory cells, and wherein the input/output control circuit couples the first primary memory cell and the first redundant memory cell to a sense amplifier via the plurality of input/output lines associated with the same block of memory cells.